Fractal electronic devices: simulation and implementation

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Abstract. Many natural structures have fractal geometries that exhibit useful functional properties. These properties, which exploit the recurrence of patterns at increasingly small scales, are often desirable in applications and, consequently, fractal geometry is increasingly employed in diverse technologies ranging from radio antennae to storm barriers. In this paper, we explore the application of fractal geometry to electrical devices. First, we lay the foundations for the implementation of fractal devices by considering diffusion-limited aggregation (DLA) of atomic clusters. Under appropriate growth conditions, atomic clusters of various elements form fractal patterns driven by DLA. We perform a fractal analysis of both simulated and physical devices to determine their spatial scaling properties and demonstrate their potential as fractal circuit elements. Finally, we simulate conduction through idealized and DLA fractal devices and show that their fractal scaling properties generate novel, nonlinear conduction properties in response to depletion by electrostatic gates.

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Fractal geometry has been employed to describe a broad collection of physical objects, ranging from clouds, trees and coastlines through to physiological structures such as neurons, retinal nerves, bronchial trees and blood vessels [1, 2, 3]. The pervasiveness of fractals in nature can be understood in many cases by considering the advantageous properties that result from the fractal object's repetition of patterns over many size scales. These properties include the high physical connectivity between two merging fractal patterns, the ability of fractal objects to efficiently disperse energy, and their large surface area to volume ratios. Such properties have made artificial fractal structures the subject of increasing fundamental research (e.g. optical transmission [4], quantum interference [5], and mesoscopic electron transport [6]) and technological applications (e.g. capacitor [7] and antennae [8] designs).

Our prior research of 'fractal electronics' focused on impurity-induced electron scattering, which caused the electrons to flow through micro and nano-scale devices along fractal trajectories [73, 129, 188]. In this paper, we propose a more controlled way of generating fractal electricity in which novel electronic devices feature a fractal distribution of conducting channels. We will focus on devices formed from atomic clusters of metallic elements that 'self-assemble' on flat surfaces as a candidate for future implementation of these devices. This process is based on a modified form of diffusion-limited aggregation (DLA), which is known to generate fractal structures in which branch-like patterns repeat at different size scales [9]. Self-assembly has the advantage of minimizing the waste of material inherent in traditional fabrication techniques. It also enables the efficient generation of whole arrays of complex, multi-scale structures in a single deposition step.

We will show that the size, shape and fractal properties of the branched structures can be controlled by their growth conditions. In particular, the magnification range over which fractal

scaling occurs can be tuned, providing the ability to adjust the relative contributions of coarse scale and fine scale branches to the structures. The resulting changes allow the boundary lengths of the individual branched structures to be maximized, leading to a greater physical and electrical connection between the neighboring structures that link together to form one type of fractal device.

In addition to such structural advantages of the fractal devices, we propose that the underlying geometry might be further exploited to generate inherent non-linearities in the electrical conduction properties of the devices. We use simulations to demonstrate novel conduction behavior induced by electrostatic gates that selectively route current through the fractal distribution of conducting channels of the device. To demonstrate the potential of fractal devices, we will present simulations of two families of device designs - one in which the patterns repeat exactly at different size scales ('exact' fractals) and one in which the statistical properties of the patterns repeat ('statistical' fractals). We will show that both display non-linear transport behavior generated by their underlying fractal geometry and that these non-linearities can be tuned to be larger than those observed in non-fractal devices.

1. The Fractal Properties of DLA Patterns

The formation of our candidate fractal patterns is based on classical diffusion-limited aggregation (DLA) of atomic clusters. In DLA simulations, particles are released from a boundary on the substrate and diffuse freely until they encounter a stationary particle fixed to the surface. Once this encounter has occurred, the particle has its position fixed and the process is repeated [9]. Figure 1(a) shows a simulated pattern or 'island' generated from approximately 100,000 particles. This DLA island displays the fractal patterning created by the repetition of structure across many size scales.

However, for DLA islands formed from self-assembly processes such as atomic cluster deposition, this simple model is inadequate to describe the physics involved. In Figure 1(b), we therefore present a pattern generated by a kinetic Monte Carlo simulation [10], in which multiple particles are allowed to impinge anywhere on the substrate (as if from a beam of atomic clusters [11-15]) rather than single particles released from a boundary. This diffusion model is based on a model described in [16]. In addition, we can tune the relative rates of particle deposition, and particle diffusion along the edges and corners of the island. Each of these describes a process that occurs during the deposition of atomic clusters on a substrate and their presence has the effect of smoothing out the finest branches as Figure 1(b) demonstrates [11].

The Monte Carlo simulation generates a structure intermediate between that produced by classical DLA and the physical example of self-assembled fractals that we will be considering in this paper, antimony (Sb) clusters deposited on atomically-flat substrates [11]. To facilitate a visual comparison of the simulated islands with the grown Sb islands, in Figure 1(c) we have traced out the boundary edge (in black) of one of the Sb islands. We have also included a 'backbone' pattern (in red) to highlight the coarse scale structure. Whereas the coarse scale structure of the grown Sb island is visually reminiscent of the DLA simulation, the island's edge clearly lacks the first simulation's fine structure (Figure 1(a)). This absence of fine structure is due an increased prevalence of the particle diffusion effects included in the Monte Carlo simulation [10,17].

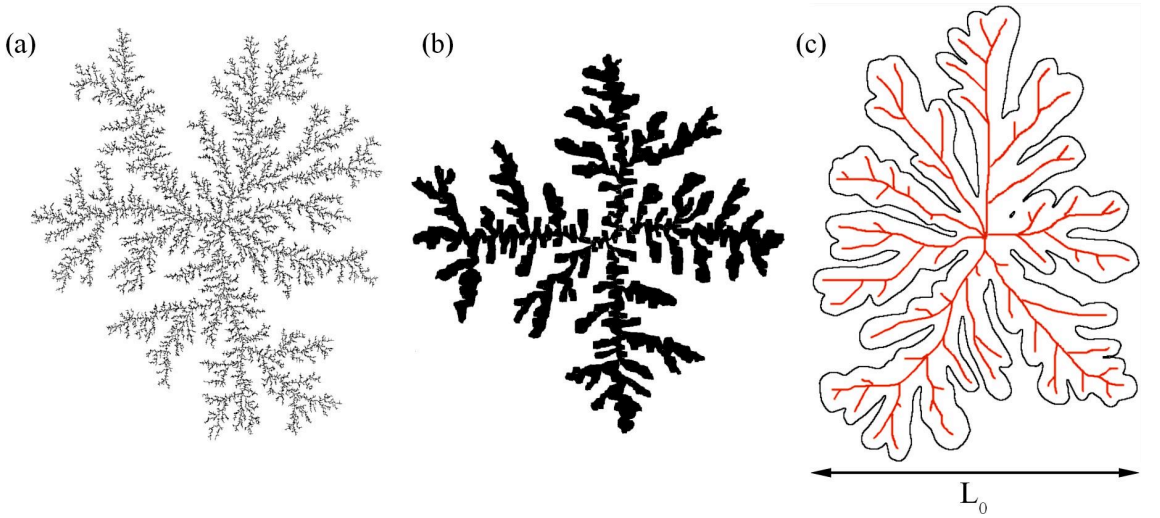

Figure 1. (a) A simulated DLA pattern, (b) a simulated island with edge diffusion and coalescence of clusters included in the DLA model, (c) a Sb island [11]. The island's boundary edge is shown in black and the 'backbone' branching structure is shown in red. The island width in (c) is $L_0 \approx 2.2$ μm.

Self-assembled, fractal patterns have previously been observed in a variety of metallic systems under a range of growth conditions [12,13,18]. While utilization of more highly branched structures similar to those shown in Figure 1(b) is certainly possible [11-13,18], here we focus on less highly branched structures such as those shown in Fig 1(c). The reason for this is that, in real systems, some edge diffusion is likely and it is therefore important to investigate the range of structures that is realistically obtainable (this range of structures is discussed in more detail below). These structures can be prepared, for example, by depositing high purity (99.998%) Sb_4 clusters on highly-oriented pyrolytic graphite (HOPG) in an ultra high vacuum, which results in highly branched Sb patterns [11]. Figure 2(a) shows a schematic representation of the fabrication process, which employs thermal evaporation to generate and deposit a beam of atomic clusters on a substrate. Figure 2(b) shows an example SEM image of Sb 'islands' deposited on the substrate at a rate of 0.2 Å/s.

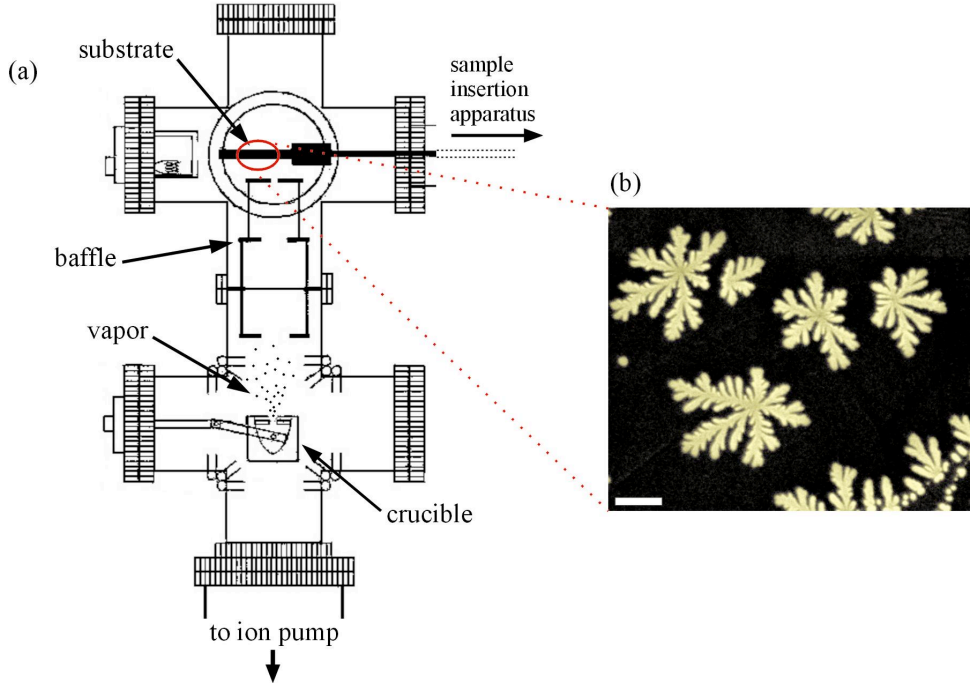

Figure 2. (a) A schematic representation of the UHV setup used to fabricate the Sb islands, (b) a SEM image of Sb islands for which the mean thickness was 10 monolayers. The scale bar corresponds to 1 μm.

How do these growth processes affect the fractal properties of the islands? We investigate this question by applying a traditional fractal analysis known as the 'box-counting' method [19] to the edges of the islands. Using this technique, the edge pattern is covered with a computer-generated mesh of identical squares (or 'boxes'). The number of squares, $N(L)$, that contain any part of the edge pattern is then counted, and this count is repeated as the size, L, of the squares in the mesh is reduced. $N(L)$ gives a measure of the space coverage of the pattern, and reducing the square size is equivalent to looking at this coverage at finer magnifications. For fractal behavior, $N(L)$ scales according to the power law relationship $N(L) \sim L^{-D}$, where $1 < D < 2$. This power law generates the scale-invariant properties that are central to fractal geometry and manifests itself as a straight line in the 'scaling plot' of $\log(N(L))$ versus $\log(L)$, as shown in Figure 3 for the three patterns of Figure 1. To allow direct comparisons between the size scales of the three islands, the L values are normalized to the overall scale of the island, L_0.

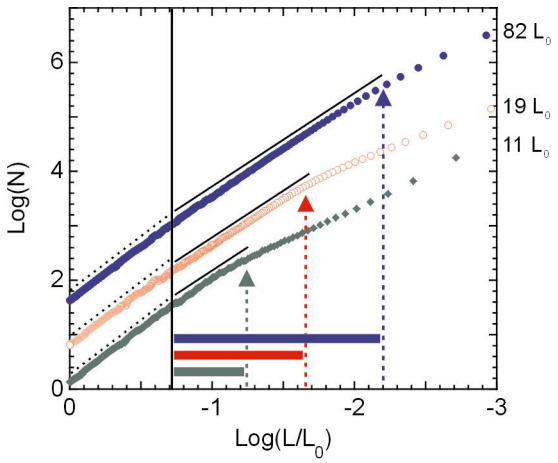

Figure 3. The box-counting analysis for the simulated DLA island of Figure 1(a) (blue circles), the modified-DLA simulated island of Figure 1(b) (open red circles), and the grown Sb island of Figure 1(c) (green diamonds). The bars and arrows in the corresponding colors indicate the extent of each island's fractal scaling range. In those scaling ranges, black lines indicate the $D = 1.7$ gradient. Outside the fractal scaling range, D converges towards 2 at large box sizes where all boxes contain part of the island, and D converges towards 1 at box sizes smaller than the finest features of the island. The dotted lines on the left of the plot indicate $D = 2$. The perimeter of each pattern is also indicated at the fine scale end of the plot.

These scaling plots are important for quantifying the factors that generate the favorable functional characteristics of fractal objects. In particular, the large physical (and therefore electrical) connectivity between two fractal devices arises from the repetition of spatial structure mapped out by the scaling plots, and these characteristics can be enhanced by adjusting two crucial factors. The first factor is the power law exponent D, which represents the boundary's dimension and describes how the patterns occurring at different magnifications combine to build the resulting fractal shape. Since D corresponds to the gradient of the scaling data, it charts the 'rate' at which structure is added as we magnify an edge: a high fractional D value corresponds to a higher rate, which leads to a higher ratio of fine to coarse structure in the pattern. The second factor is the magnification range over which this fractal scaling occurs and this is set by coarse and fine scale cut-offs between which lies a constant, fractional D[a].

The scaling plots of Figure 3 allow an investigation of how the differing growth conditions of the islands of Figure 1 impact on their D values and their magnification ranges. The D value for the simulated island of Figure 1(a) matches the well-established value for DLA of 1.7 [9]. This scaling 'rate' is preserved for all three islands (see Fig. 3), indicating that the changing growth conditions have not modified the basic particle dynamics of the fractal generation process: all three islands are formed from a DLA process. However, the changing growth conditions have reduced the magnification range over which the fractal scaling holds, as illustrated by the colored

[a] Note that in the box-counting method, two effects are always present and can be clearly seen in our scaling plots. At large box sizes, the gradient (D) will approach 2 as the boxes become sufficiently large that a part of the pattern is in every box (*i.e.* all boxes are filled). At the small box scale, once boxes become small enough to fit inside the line representing the edge of the pattern, D will tend toward 1. These conditions set the measurement limits of the fractal analysis and are referred to as the coarse and fine observation 'cut-offs' respectively.

bars at the base of the scaling plot. This corresponds to a gradual suppression of fine scale branching by edge diffusion and cluster coalescence. To emphasize the importance of this reduction of magnification range on functional properties, we have measured the perimeter lengths of the three islands. The pure DLA island of Figure 1(a) has a perimeter of $82L_0$, and this is reduced to only $11L_0$ in Figure 1(c). This reduced perimeter length impacts on functional properties such as the connectivity between two islands.

The Sb island of Figure 1(c) scales over approximately 0.5 orders of magnitude (too small a magnification range to be considered strictly fractal). For our proposed fractal electronic devices, it is therefore informative to consider the potential for increasing this fractal scaling range. It has been shown previously that the island growth conditions can strongly affect the structure of the islands. By increasing the deposition rate [11], island size (see below), cluster size [20], or decreasing the substrate temperature [21], the islands develop more fine structure. This decrease of the fine scale 'cut-off' increases the fractal scaling region and thus the islands' effectiveness as fractal electronic circuit elements. The fractal scaling range can also be extended by increasing the coarse scale cut-off, achieved by growing larger islands (as measured by the island scale L_0). Depositing more material, as shown sequentially in Figure 4(a, b, c) for 5 monolayers (ML), 10 ML, and 40 ML respectively, results in larger, more highly branched structures with correspondingly larger fractal scaling ranges.

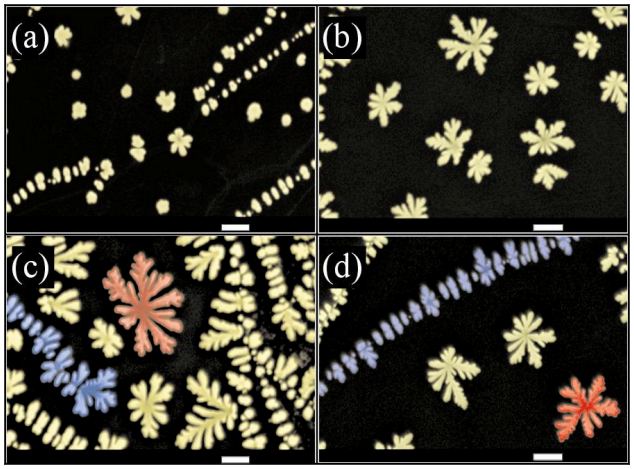

Figure 4. (a), (b), and (c) show SEM images that demonstrate the growth of the islands at a constant (0.03 Å/s) deposition rate with 5, 10, and 40 effective monolayers on the substrate respectively. The images in (c) and (d) show the two typical types of island nucleation: that due to collisions between Sb_4 clusters on the flat HOPG terrace (examples colored red) and that due to aggregation at step edges on the HOPG (examples colored blue) [11]. Scale bars correspond to 1 μm.

Crucially, there are physical constraints on both the minimum and maximum values for the island diameter L_0. The minimum size of a branched island is dictated by the so-called 'critical radius' (r_c) of the island. r_c is the size at which an island will transition from a compact, circular shape to a more branched structure. This transition can be measured by exploiting the fact that it is accompanied by a change in the mathematical relationship between the perimeter of the island and the area that it encloses [11]. The transition is determined by the analysis shown in Figure 5, where the knee in the data indicates the transition from circular island geometry (with a

smooth perimeter and $D = 1$) to a branched structure (with a larger perimeter and $D = 1.7$). This minimum island size can be decreased significantly by depositing material at a faster rate [11].

The maximum possible island size is set primarily by the distance between neighboring islands. On flat HOPG terraces, this distance can be controlled by the initial cluster deposition rate and the prevalence of substrate surface defects. The deposition rate controls the number of clusters that are diffusing on the substrate at one time. A higher deposition rate corresponds to more diffusing clusters and thus a greater possibility of clusters colliding and forming a nucleation point for an island. Depositing more slowly reduces the density of islands, increasing the average maximum island size. Examples of this type of island nucleation (i.e. from cluster collision) are highlighted in Figure 4(c) and (d) in red. Surface defects (i.e. any feature that disturbs the flatness of the substrate) can also cause island nucleation. For instance, a step edge in the substrate promotes island growth radiating from the edge, as highlighted in blue (Figure 4(c,d)). On an HOPG substrate, the step edge density depends dramatically on the quality of substrate and varies randomly at different locations. The density of random defects such as impurity adatoms can be reduced to a level at which they are negligible by using standard thermal annealing and crystal cleaving procedures [11]. We note that while HOPG has been used as a substrate in our earlier work, similar structures are obtained through diffusion on other atomically flat substrates such as MoS_2 and mica.

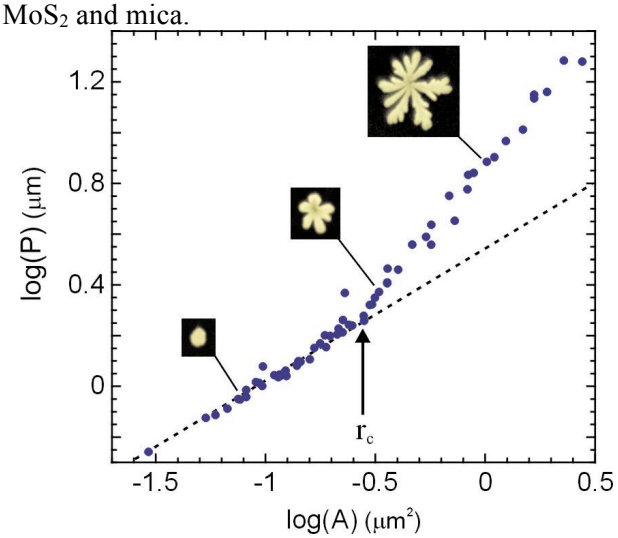

Figure 5. A plot of log (island perimeter) vs. log (island area), as measured from a digital SEM image. Each data point represents an individual island. All islands, of varying sizes, are grown under identical conditions. The dotted line is a guide to the eye, showing the behavior expected for purely ellipsoidal (i.e. non-fractal) islands. The critical radius (r_c) represents the point at which the data deviates from this behaviour, indicating the formation of branches.

The ability to manipulate surface features will therefore be central to future device designs: for example, for connecting the islands to source and drain electrodes. We anticipate that focused ion beam (FIB) milling will be optimal for patterning more precise and intricate artificial nucleation sites. FIB features have previously been shown to act as artificial nucleation sites for the islands [22,23]. Standard lithography techniques can also be used to define boundaries restricting the islands to selected substrate regions so that they do not merge with other circuit components.

The material used to assemble the devices is also an important consideration. Semimetallic materials such as Sb and Bi allow some control of their carrier concentration by gating, but it may be preferable to create the fractal structures described in this paper by deposition of semiconducting clusters such as Si and Ge. A promising alternative is to deposit Sn clusters, and deliberately oxidize the resultant fractal structures to convert them to semiconducting $Sn0_2$ [24]. It has recently been demonstrated that nanowire devices can be fabricated by similar methods [14].

Finally, we consider the substrate material for the proposed fractal electronic devices. In principle, these islands could be deposited on any atomically flat substrate, i.e. one where impinging clusters experience a relatively featureless energy profile, enabling them to diffuse. In practice, HOPG is often used, but has the drawback of being a conductor ($\sigma \approx 4 \times 10^{-7}$ Ω·m) in the plane parallel to its surface. An insulating substrate such as mica, MoS_2 or epitaxially-grown silicon nitride will be required for our electronic devices. Alternatively, the adhesion of the fractal islands to the HOPG surface is quite weak [11], which may enable post-deposition contact transfer of the islands from the original HOPG substrate to a more strongly attracting, insulating substrate [25].

2. Conduction Properties of Fractal Devices

Implementation of the above material growth and fabrication techniques will allow the design of a variety of device architectures with properties related to the fractal geometry of the constituent islands. In the previous section, we noted that the two scaling parameters of fractals – the *D* value and scaling range – will determine the device's structural properties, including the physical and electrical connection between two neighboring islands. These two parameters are also expected to determine the distribution of electrical current through the branches of an individual island. It should be possible to manipulate this current by using electrostatic gates to deplete selected regions of the device. The locations and shapes of both the electrodes and the gates can be chosen to maximize electrical connections to the fractal circuit element. Figure 6 shows two possible configurations each based on single islands, where the truncated circle drain (green) connects to many of the branches of a single simulated DLA pattern. Gates (symbolized by blue arrows) adjacent to the source electrode (red) could then be used to incrementally reduce the number of connections to the drain, routing current through the remaining branches.

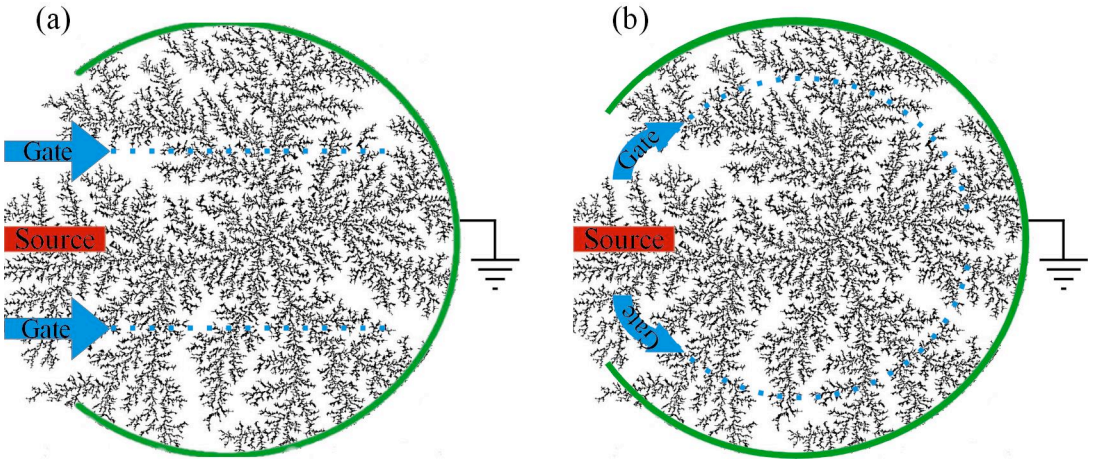

Figure 6. Schematic representations of two gating schemes for a DLA pattern: (a) a simple, plunger gate configuration and (b) a series of gates creating an arching depletion pattern. Current flows through the fractal island from source (red) to drain (green), routed by the electrostatic gates (blue), which would deplete the structure along the dotted paths.

The gating scheme shown in Figure 6(b) was chosen to match the radial symmetry of the pattern, not for its ease of implementation. Electrostatic gating around such an arc would require a large number of independent top gates that could be switched on sequentially, each forming a small linear part of the overall arc shape. Considering the physical size (~ 3 μm in diameter) of the proposed circuit elements, this may prove challenging to achieve. Figure 6(a) shows an alternative design which will be simpler to implement but which would have more limited flexibility in terms of selective depletion of the fractal branches.

For such fractal devices we need to examine how the gates can be employed to transfer the inherent nonlinearity of the fractal's spatial geometry into novel nonlinear features in the device's gate characteristics. We begin by focusing on fractals where the pattern repetition at different magnifications is exact (so-called 'exact' fractals). These fractals are relatively simple compared to 'statistical' fractals, generated by processes such as DLA, where only the statistical properties of the patterns repeat at many scales. This simplicity allows correlations between a device's spatial geometry and the resulting gate characteristics to be more easily identified. Nevertheless, the scaling properties of statistical and exact fractals depend on D in the same manner, such that generic properties that are dependent on D for exact fractals should be readily transferable to statistical patterns such as the self-assembled DLA devices. We will return to a demonstration of this for DLA devices later in the paper.

To explore a wide variety of possible device architectures, we developed a simple device simulation program based on the modified nodal analysis technique [26]. The program takes as the input an image of the desired device architecture in the color scheme shown in Figure 6 (source = red, drain = green, resistors = black, perfect insulators = white). The exact solutions to the resulting matrix are obtained via Mathematica's standard linear system solver and give the voltage at every pixel (i.e. circuit node) as well as the total current flowing to the drain. With these quantities and a fixed voltage applied to the source, it is simple to calculate the resistance of an arbitrary pattern. It is important to emphasize that this method solves a *classical* resistor network. Quantum effects like conductance quantization, electron wave interference, and

tunneling, which may become important as the device size is reduced, will offer rich opportunities for future investigations of these devices.

Figure 7(a) shows two iterations of an exact fractal known as the Sierpinski carpet [27]. This fractal pattern was chosen for our studies because its high D value (= 1.89) is similar to that of DLA-based devices. For the Sierpinski device, square patterns (shown in white in Figure 7(a)) repeat at different size scales, at a rate determined by D. These squares represent insulating regions and therefore create a fractal distribution of conducting channels (black regions in Figure 7(a)), analogous to the fractal branches of the islands discussed earlier. Current passes through these channels from the source (red) to drain (green) electrodes, routed by a pair of narrow electrostatic side-gates. Two gate architectures are investigated: a pair of symmetric gates positioned to be level with the central square of the device (i.e. with positions indicated by the two blue arrows in Figure 7(a)) and a pair of symmetric gates with positions offset from the central square (red arrows). The blue and red 'depletion' boxes in Figure 7(a) show the regions of the device over which depletion occurs due to a voltage applied to the gates at the indicated positions. As the voltage applied to the gate is increased, the depleted region penetrates further into the structure. The depletion distance, x, (measured from the edge of the pattern at the arrow positions) is measured in microns. We have chosen the smallest current-carrying channel to be 50nm wide (achievable in practice with electron beam lithography) meaning that the entire device is 1.35 microns wide.

For clarity, Figure 7(b) shows the patterns inputted into the simulation for depletions corresponding to x = 50 nm and x = 350 nm in the case of the centrally located gate pair. Similar patterns (x = 0, 50, 100, ..., 450, and 500 nm) are simulated to generate Figure 7(c), which shows the resistance and differential resistance (R and dR/dx) curves for the 2 iteration Sierpinski device as a function of the gate-induced depletion. Depleting the current-carrying channels (black) causes a series of dR/dx responses whose amplitudes are set by the width of the remaining conducting channels and the width of the adjacent white square, but whose occurrence (i.e. position along the x axis of Figure 7(c)) is dictated entirely by the fractal geometry of the device.

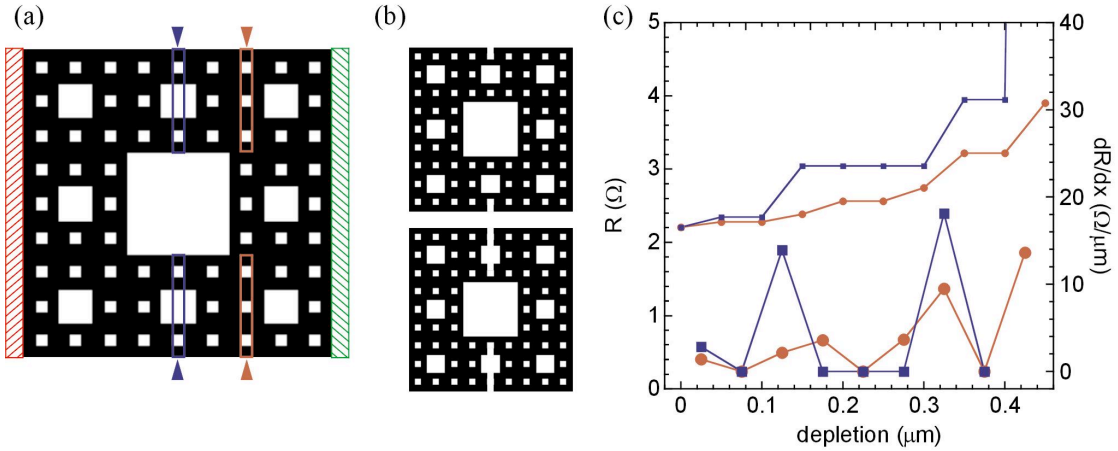

Figure 7. Architecture and simulation results for a 2-iteration Sierpinski device. (a) The device architecture has broad source (red bar) and drain (green bar) electrodes on either side of the device. The positions of the two different gate configurations are indicated with pairs of arrows, and the maximum extent of the gating

is shown by the boxes in matching color. (b) Two examples of depletion for the central gate pair, corresponding to the data points for 50 and 350 nm depletion in (c). (c) The results of the device simulations are shown in terms of resistance R (upper traces) and dR/dx (lower traces) each plotted as a function of depletion distance x. The center gate (blue) and offset gate (red) configurations correspond to the appropriately colored traces.

For instance, consider the jump in resistance between the 100 and 150 nm gate depletions on the blue curve (central gate). This corresponds to depleting the third 50 nm block from the edge of the pattern, which is a conducting channel (colored black). Because that channel is immediately adjacent to the 150 nm white square in the pattern, depleting it causes all current to be forced through the two 50 nm channels closest to the large central white square, causing a significant rise in the electrical resistance of the pattern. This is followed by the 200, 250, and 300 nm depletions, which have no effect on the pattern resistance because they are within the 150 nm white square. Note that, in this instance, and in the instance between 300 and 350 nm depletion, we see a significant response in R and dR/dx for a relatively small change in depletion (i.e. gate bias).

To investigate the role of the *extent* of fractal scaling on conduction properties, we also consider the 4 iteration Sierpinski device shown in Figure 8. For this 4 iteration device, the narrowest channels in the device are again set at 50 nm wide and the device width is now 12.15 microns, compared to the 1.35 micron width of the 2 iteration device. We note that the limited fractal magnification range of the 2 iteration device (Figure 7) approximates to that of the state of the Sb structure shown in Figure 1(c). For the 4 iteration device, the fractal scaling range approximately matches that of the simulated DLA pattern in Figure 1(a).

In the 4 iteration device simulations, the narrow gates have the same positions as for the 2 iteration device, although now, because of the increased width of the device, they deplete along a line that is 9 times as long (Figure 8(a)). The occurrence (along the x axis of Figure 8(b)) of the resistance features is once again dictated by the fractal geometry of the device. However, the increase in iterations leads to a far more complex differential resistance response (Figure 8(b)), which highlights the sensitivity of the dR/dx features to the widths of the undepleted channels and the adjacent fractal features of the device. More specifically, we see (as with the 2 iteration Sierpinski device) large dR/dx peaks when the channels being depleted are adjacent to large features, i.e. large white squares. The size of the peaks is therefore linked to the size of the squares in the proximity of the depleted channels and, in particular, to the proximity of the central square. The latter dependency is intuitive, but can be seen quantitatively in Figure 8(b) by comparing, for instance, the relative peak size at x = 450 nm and x = 3150 nm. In each case, the channels being depleted are adjacent to a 450 nm wide square, but at x= 3150 nm there is an enhanced response due to the proximity of the channels to the central square.

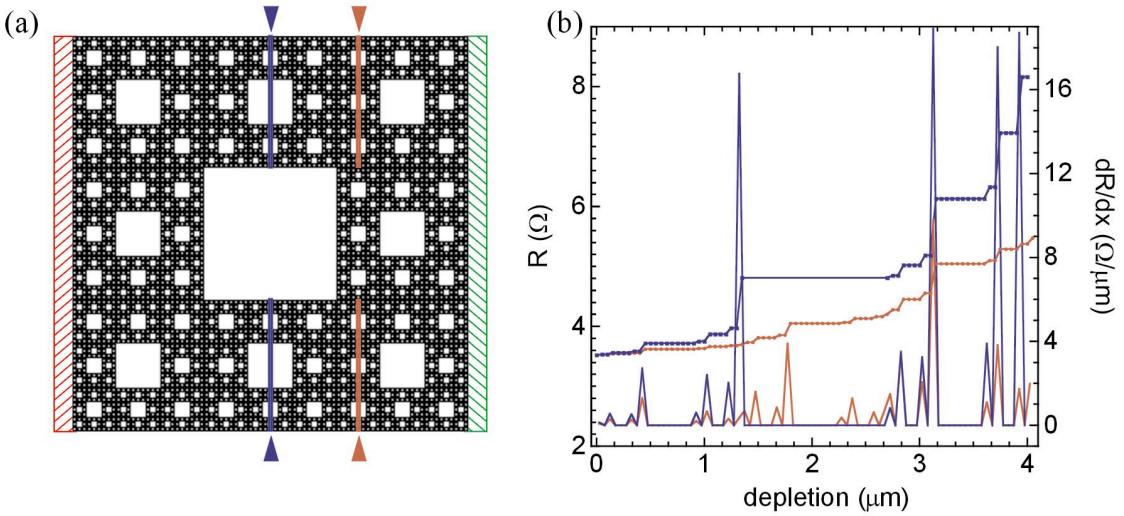

Figure 8. Architecture and simulation results for a 4 iteration Sierpinski device. (a) The device architecture has broad source (red bar) and drain (green bar) electrodes on either side of the device. The positions of the two different gate configurations are indicated with pairs of arrows, and the depletion region of the gating is shown in matching color. (b) The results of the device simulations are shown in terms of resistance *R* (upper traces) and *dR/dx* (lower traces) versus depletion distance *x* measured in microns. The center gate (blue) and offset gate (red) configurations correspond to the appropriately colored traces.

Further complexity in the differential resistance can be induced by employing gates that span the entire length of the device from source to drain (Figure 9(a)). The results of this gate configuration for the 4 iteration device are shown in Figure 9(b) (black curve). The full width gates clearly add features to the *dR/dx* curve of the device. The relationship between the *dR/dx* response and the underlying fractal structure is now more subtle: as indicated, the full length gate is equivalent to a combination of line gates addressing every point along the device between source and drain, leading to the simultaneous depletion across many device features. In terms of the positions of the *dR/dx* peaks, the full length gate can be thought of as a superposition of all possible 50 nm length gates. This idea is illustrated by comparison to the two 50 nm gate *dR/dx* curves from Fig. 8 (blue and red in Figure 9(b)).

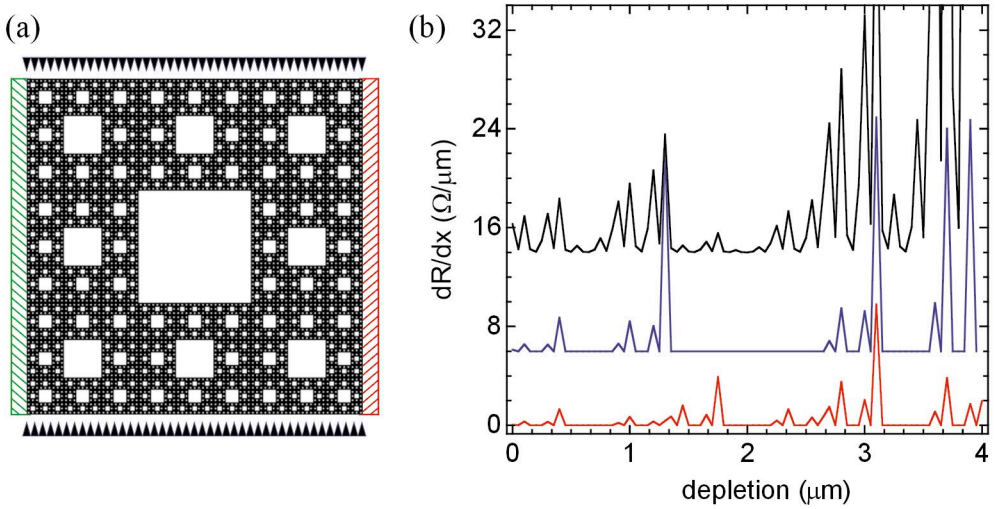

Figure 9. A comparison of a Sierpinski device (4 iteration) for three different gate configurations. (a) The full length gate is shown schematically, and is essentially a combination of minimum length (50 nm) gates at every position across the pattern. (b) The *dR/dx* curves for the offset gate (red), centered gate (blue), and a full length gate (black) on the 4 iteration Sierpinski device.

To further demonstrate the unique properties of a fractal device pattern, we consider a control device: a non-fractal, but still finely-featured, pattern. In order for the comparison to be informative, the large-scale features of the control device should match those of the Sierpinksi device. Figure 10(b) shows a selected pattern, which retains the large central square of insulating material so that the background increase in *dR/dx* has the same trend as the 4 iteration Sierpinski device of Figure 8(a). The fractal structure around the central square is replaced with a grid of identically-sized, 50 nm, white squares, which can most easily be seen in the magnified portion of Figure 10(b). Simulated *dR/dx* results (Figure 10(c)) for both the control (Fig 10(b)) and fractal (Fig. 8(a), which is repeated as Fig. 10(a)) patterns show that the fractal has enhanced response to small changes in depletion.

The interesting characteristic of the Sierpinski device's *dR/dx* response lies in its repeated pattern of enhanced *dR/dx* over the whole range of depletions. The Sierpinski device (Figure 10(a)) produces larger features in *dR/dx* over selected depletion regions, which translates to a more sensitive response to gating than the control device. This sensitivity over certain depletion regions is potentially very useful in a wide range of applications, as described in the Conclusions section below.

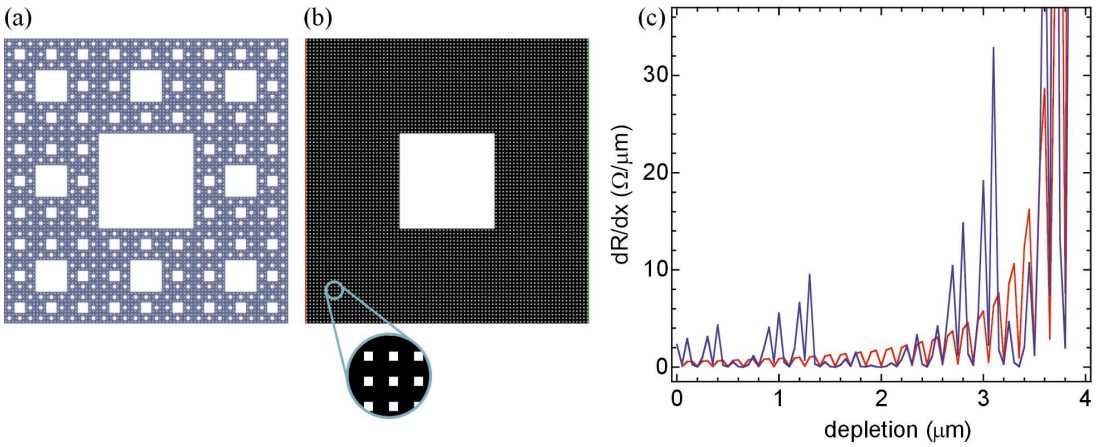

Figure 10. (a) the Sierpinski device (repeated from Fig 8(a) to allow comparison with (b)) and (b) the non-fractal control device. (c) *dR/dx* of a Sierpinski device (blue trace) compared to that of the non-fractal device (red trace). Both traces are generated for the full length gate.

Fractal devices based on exact repetition (such as the Sierpinski devices shown above) could be fabricated using traditional lithography techniques such as electron-beam lithography. However, self-assembly is a more practical approach to fabricating devices featuring many levels of iteration. Lastly, therefore, we return to the self-assembled DLA-based fractal device shown in Figure 6. Simulations of these devices have *R* and *dR/dx* results, shown in Figure 11, that have fractal-induced non-linearities analogous to the Sierpinski device's responses. This is encouraging for future implementations of diffusion-limited aggregate-type devices for applications based on non-linear responses.

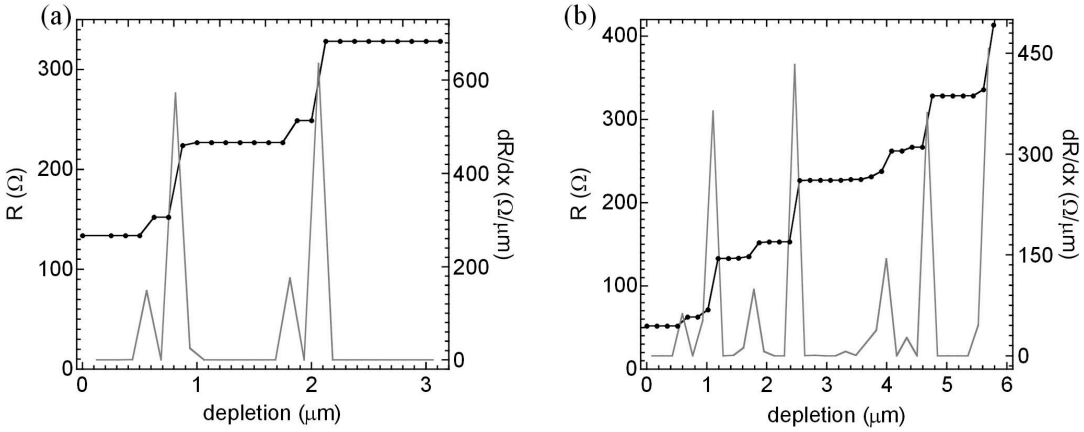

Figure 11. Simulation results for DLA devices in two gating configurations with *R* (black) and *dR/dx* (gray) displayed. The labeling (a, b) is the same as for Figure 6. Note the units of depletion are the same for the two graphs, though in the case of (b), depletion is an arc length due to the gate geometry.

3. Conclusions

Fractal geometry is prevalent in a wide variety of natural and manufactured devices and provides many functional advantages over more conventional, Euclidean systems. In this paper, we proposed extending fractal geometry to micron-scale electronic devices and identified self-assembled nanocluster systems as a flexible platform for such studies (although as noted earlier, similar geometries can also be engineered by standard lithographic methods). These systems assemble devices with branch-like patterns that repeat across a range of size scales.

We considered how the growth properties of these systems could be adjusted to tune the fractal characteristics of the devices formed from the branch structures. In particular, the fractal-scaling magnification range could be adjusted, leading to the ability to dictate the relative contributions of coarse scale and fine scale branches to the overall pattern. We proposed that this underlying geometry might be further exploited to generate inherent non-linearities in the electrical conduction properties of the devices.

To explore the electrical characteristics of fractal circuit elements, we developed simulations that we used to demonstrate novel, non-linear conduction behaviors generated by employing electrostatic gates. Small, incremental changes in the gate bias showed comparatively large responses in the electrical resistance of the device. Furthermore, increasing the fractal scaling range of the device dramatically increased the variety and size of these non-linearities.

In terms of applications for these interesting electrical characteristics, we note that one of the key figures of merit in standard MOS transistors is the transconductance (i.e. dI_{sd}/dV_g), which gives the change in the output of the device (the source-drain current, I_{sd}) as a function of the input to the device (the applied gate voltage, V_g). A large transconductance implies that a large output signal can be obtained from a small input signal, and thus the transistor works as a high gain amplifier.

The quantity dR/dx calculated for the fractal devices in the last section is equivalent to the transconductance in a conventional transistor, since the depletion, x, is a function of the applied gate voltage. We note that dR/dx varies dramatically (see Figure 9) over a range of gate voltages, and it is not therefore immediately clear how this behavior can be used directly in a transistor. However, there are a wide range of MOSFET-based sensors which operate on the same principles as a transistor: charge induced on a gate by an arriving molecule (the analyte) induces a change in carrier concentration in the channel of the MOSFET, and hence a change in current, which allows the arrival of the molecule to be detected. In FET devices based on nanowires it has been shown that it is possible to detect *single* molecules of a range of analytes, including gases and viruses [28]. In these devices, the transconductance is a measure of the sensitivity of the device to the analyte, but it is not essential for the transconductance to be constant (or even large) for all applied gate voltages. We anticipate that the present fractal electronic devices could be used as high sensitivity sensors by tuning the applied gate voltage to a peak in dR/dx. The arrival of the analyte would then cause depletion of the next narrow channel in the device, enabling its detection.

We hope that these results will trigger further theoretical and experimental interest in fractal electronic devices and their potential applications. In addition to the electronic gating functionality discussed in this paper, fractal devices have potential within the growing field of biomimicry in which artificial structures are based on functionalities found in nature. For example, the self-assembled fractal devices discussed here could be exploited in artificial retinas to serve as biophilic interconnects between photodiodes and the fractal nerves in the retina [29]. Alternatively, the devices could be employed in novel solar cell architectures that use the fractal

devices as electrodes that more efficiently extract carriers from the photoactive material. In these and other applications, the structural and electrical properties of the fractal devices will be central to their operation.

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